55. A method for driving one of a plurality of pixels of a display as claimed in Claim 54, wherein the display is one of a liquid crystal display, an electroluminescence display and a field-emission display.

**In the Drawings**

Formal drawings are being submitted concurrently herewith.

**Remarks**

**Election/Restrictions**

1. The examiner has requested affirmation of Applicants' election to prosecute the invention of Group I, namely Claims 1-35, 54-55 and 58-61. That affirmation is hereby provided.

**Information Disclosure Statement**

4. The examiner states that the IDS filed on July 21, 2000 (Paper No. 5) is missing from the application file. The examiner has requested that the IDS and the references listed therein be resubmitted. This is being done concurrently with this Amendment, along with a Supplemental IDS that discloses additional information.

5. The examiner states that he was unable to find a legible copy of each of the non-patent documents listed on the Information Disclosure Statement that applicant filed on March 14, 2000 (Paper No. 4). Applicants submit herewith replacement copies of these documents.

**Drawings**

6. The examiner objects to the drawings filed on September 3, 1999, because of problems found by the Draftsperson as described on the attached form PTO 948. The examiner states that corrected drawings are required. Applicants have provided corrected drawings, as set forth on the enclosed Submission of Formal Drawings.

7. The examiner has objected to Figure 2 of the drawings because of a spelling error and states that the reference character for element 115 should be changed to -- Recovery Connection System -- instead of "Recovery Conection System" (emphasis in original). The examiner states that a proposed drawing correction or corrected drawings are required. The corrected drawings that accompany the Submission of Formal Drawings make this correction.

8. The examiner has objected to the drawings under 37 C.F.R. § 1.83(a). The examiner states that the drawings fail to show the "other capacitances" that are referred to in Claims 1, 25 and 58, and the "other capacitance-generating components" that are referred to in Claim 44.

With respect to the "other capacitances," these are stray capacitances caused by such elements as the column driving lines 73 and 79 and the gate capacitances of the non-selected FETs 49 and 53 shown in Fig. 1. These collective capacitances are further illustrated as a capacitor 105 in Fig. 2, as explained in the second full paragraph on page 9 of the Specification.

With respect to the "other capacitance-generating components," Applicant has withdrawn Claim 44 from consideration. Applicant has further incorporated the language of Claim 44 in amended Claim 54, but has amended the reference to "other capacitance-generating components" to read "other capacitances" for better clarity.

**Claim Objections**

9. The examiner has objected to Claims 54 and 54 as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant has amended Claim 54 to be independent. Applicant has also amended Claim 55 to now depend on Claim 54. Claim 55 further limits the subject matter of Claim 54 in that it limits the display to one of a specified type.

The examiner has also rejected Claims 54 and 55 as being dependent upon a non-elected base Claim 44. As indicated, applicant has amended Claim 54 to be independent and has amended Claim 55 to depend upon Claim 54.

**Claim Rejections -- 35 U.S.C. § 112**

The examiner has objected to Claims 54 and 55 under 35 U.S.C. § 112 because the claim limitation "other capacitance-generating components" was not described in the specification. Applicants have amended Claims 54 and 55 so that "other capacitance-generating components" now reads -- other capacitances --.

**Claim Rejections -- 35 U.S.C. § 103**

The examiner has rejected Claims 1-5, 7-9, 11-17, 19-21, 23-27, 29-31, 35 and 58-61 under 35 U.S.C. § 103(a) as being unpatentable over Orita et al. in view of Schlecht et al. This rejection is respectfully traversed.

**– All Claims Limitations Not Taught**

"To establish a *prima facie* case of obviousness . . . the prior art reference (references when combined) must teach or suggest all the claim limitations." M.P.E.P. § 2142. That is not the case here.

One key feature of the invention, as expressed in various ways in elected and independent claims 1, 13, 25 and 58, is that the energy consumed by a display is reduced by discharging the stray capacitances separately from the load capacitance, such as the capacitance imposed by a pixel in the display.

The examiner appears to concede that this feature is not taught by Orita. (The examiner states "Orita does not teach . . . recovering energy from the portion of the other capacitances without at the same time recovering energy stored in the first one of the capacitive elements . . . ." Office Action mailed July 12, 2002, at p. 6.)

The examiner nevertheless urges that this feature is taught by Schlecht. Specifically, the examiner states:

> Schlecht teaches a recovered energy circuit for driving a computer display, wherein the load capacitor C262 and the parasitic capacitances C261 (which are read on the claimed limitation: the "other capacitances")

(see FIG. 26; col. 1, lines 17-19; and col. 20, lines 7-23) are charged and discharged during respective first half cycle and second half cycle; and the recovering energy from the parasitic capacitances is at the half cycle when the load capacitor is not active (see col. 2, lines 43-60).

Applicants respectfully disagree.

Schlecht describes a technique for designing logic circuitry that retrieves energy from capacitances to effect low-power circuitry. Nowhere is there any disclosure of a power supply for a display. The terms "display", "LCD" and "liquid crystal" do not even appear in the document.

The Examiner points to the power supply circuit that is shown in Figure 26 and associates this with a section of text at column 2, lines 43-60. In fact, however, the text refers to a logic circuit shown in Figure 4A which is described more fully at column 5, lines 64 et seq.

The Schlecht logic comprises a chain of logic stages driven by an AC power supply with alternate logic stages active on positive-going and negative-going half cycles of the power supply (which also serves as a clock).

The fundamental principle of the Schlecht logic is wholly inapplicable to driving of a display because the state of one stage of the Schlecht logic is dependent upon the state of the preceding stage(s).

With reference to Figure 26, nowhere does Schlecht disclose or suggest that this power supply would be suitable for driving a display. Unfortunately, Figure 26 is not easy to understand, because it is an equivalent circuit and also because the accompanying description misquotes some key reference numerals.

The relevant part of the description of Figure 26 starts at column 19, line 54. The logic chip which is the "load" of this power supply is shown towards the top of the figure within a rectangle of dotted lines. The load is modeled by a capacitor C264 which

represents the capacitors that store logic states, diodes D263 and D264 that model the transistors and diodes, and a capacitor C261 which models parasitic capacitance. The capacitors C264 and C263 appears to have been misidentified at column 20, lines 13 through 16. The description refers to C262 when it seemingly should refer to C264; and it refers to C261 when it seemingly should refer to C263. This can be seen to be the case because the description at column 20, line 7 et seq. relates to the chip and because the capacitors C261 and C262 are symmetrical components for the positive side of the power supply and the negative side of the power supply – they must either both be parasitic or both be "real." At column 21, lines 25 and 26, they are described as the parasitic capacitances of switches SW261 and SW262.

The closest possible analogy (insofar as any analogy can be drawn) between the equivalent circuit shown in Figure 26 and the display driver circuit of the present invention is the relationship between the capacitors C264 and C263. The capacitor C264 represents the useful capacitance that stores the logic states of the circuitry. This can be compared, to a degree, to the pixel capacitances in a display. The capacitor C264 in Figure 26 does not hold logical information and is made up of parasitic capacitances (column 20, lines 19 through 24) and so can be compared, to a degree, to the column line capacitances and the gate capacitances of FETs on unselected row lines.

However, there is no disclosure in Schlecht of recovering charge back to the power supply from capacitance C263 (parasitic) without also recovering charge from capacitance C264 (logic state storage), i.e., one of the features of the present invention.

The power supply in Figure 26 is entirely unremarkable--positive going pulses are derived from the uppermost Vdc in the figure, while negative-going pulses are derived from the other Vdc by controlling the switches SW261 and SW262. Energy stored as charge on capacitive elements is moved around the circuit on the half-cycles of the power supply, but this is simple a tank circuit operation. As stated above, there is no recovery of energy only from a parasitic set of capacitances while leaving charge on "useful" capacitances intact.

Finally, the Examiner refers to a portion of Schlecht at column 5, lines 51 to 58. This is simply a general statement regarding energy recovery and has no particular relevance here.

**– Motivation or Suggestion For Combination Lacking**

A further requirement for establishing a *prima facie* case of obviousness is that "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." M.P.E.P. § 2142. Not only is a key feature of the invention missing from both of the references, but this required motivation or suggestion is also missing.

To the contrary, Orita appears to teach directly away from the invention by stating that the load capacitance and stray capacitance are charged on the rising of the pulse and discharged on the falling of the pulse. *See* Col. 12, lines 25-29.

Orita further states that the disclosed techniques cause a 90% reduction in power, see Col. 1, lines 59-61. The power-saving techniques include a high-voltage holding switch (circuit elements 1113 and 1115 in Fig. 38) and a low-voltage holding switch (circuit element 1114 in Fig. 38). These circuits hold the output of the charge recovery circuit 600 at either the high or low output potential for longer than would be possible using a resonant LC circuit alone. These power-savings features are missing from the power supply in Schlecht that the examiner urges be substituted, which would make the power supply a less attractive choice, further leading the skilled artisan away from making such a substitution.

**– Summary**

In short, neither Orita nor Schlecht teaches a key feature of the invention – discharging the stray capacitance separately from the load capacitance. There is also no suggestion or motivation for combining the teachings of these two patents in the manner urged by the examiner. To the contrary, Orita appears to directly teach away from the invention. Further, the power supply in Schlecht that the examiner urges be

substituted in Orita would likely be viewed by the skilled artisan as causing inferior results. The pending claims are simply not obvious in view of Orita and Schlecht.

**– Dependent Claims**

15. Claims 2-5, 7-9, 11-12, 14-17, 19-21, 23-24, 26-27, 29-31, 35 and 59-61 are each dependent on Claims 1, 13, 25 or 58. Each are therefore not obvious in view of Orita and Schlecht for the reasons stated above, among others.

**Allowable Subject Matter**

16. The examiner has sobjected to Claims 6, 10, 18, 22, 28 and 32-34 on the ground that these claims are dependent upon a rejected base claim. For the reasons stated above, however, the base claims should now be allowable and, accordingly, these claims as well.

**Conclusion**

For the foregoing reasons, it is respectfully submitted that this case is now in condition for allowance and early notice of the same is earnestly requested.

The Commissioner is authorized to charge Deposit Account No. 501946 for payment of any additional fees required by this response or to credit any overpayment to the account. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

January 13, 2003

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## APPENDIX: MARKED-UP VERSION SHOWING CLAIM AMENDMENTS

54. [The process of claim 44, wherein the capacitive elements form pixels of a display.] A method for driving one of a plurality of pixels of a display and one or more other capacitances that are associated with a line other than the pixels of a display comprising:

d) electrically connecting each of the plurality of pixels of a display to the line;

e) storing charge in the one of the plurality of pixels of a display through the line while each of the other of the plurality of pixels of a display is electrically connected to the line; and

f) recovering energy stored in the other capacitances while maintaining the charge stored in the one of the plurality of pixels of a display.

55. A method for driving one of a plurality of pixels of a display as claimed in Claim 54 [The process of claim 44], wherein the display is one of a liquid crystal display, an electroluminescence display and a field-emission display.